IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor	:	Chen-Wen TSAI	
Appln. No.	:		
Filed	:	August 23, 2001	Group Art Unit: 2841
Title	:	MULTI-LAYERED SUBSTRATE WITH A BUILT-IN CAPACITOR DESIGN AND A METHOD OF MAKING THE SAME	Examiner: J. Gaffin
Docket No.	:	S841.312-0003	

PRELIMINARY AMENDMENT

Box Patent Applications
Assistant Commissioner for Patents
Washington, D.C. 20231

SENT VIA EXPRESS MAIL

Express Mail No.: EL800727166US

Sir:

Prior to calculation of the filing fee and examination of the application, please amend the application as follows:

IN THE SPECIFICATION

Please add the following paragraph at page 1, line 5:

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a Divisional of and claims priority, under 35 U.S.C. §120, from Application Serial Number 09/571,242 filed on May 16, 2000, entitled "MULTI-LAYERED SUBSTRATE WITH A BUILT-IN CAPACITOR DESIGN AND A METHOD OF MAKING THE SAME."

IN THE CLAIMS

Please cancel claims 4-6 without prejudice, and amend claim 1 such that pending claims 1-3 are as follows (marked up version attached in Appendix):

1. (Amended) A method of manufacturing built-in capacitors in a multi-layer substrate, said method comprising:

forming a plurality of via holes in said multi-layered substrate, said multi-layered substrate comprising a first dielectric layer, a second dielectric layer, and a third dielectric layer, said second dielectric layer having two second conductive layers being respectively mounted on a top and a bottom surface to pattern as power plane and ground plane, said first dielectric layer, and said third dielectric layer having respectively a first conductive layer and a third conductive layer;

filling a capacitor dielectric material into a portion of said via holes, which are predetermined design as capacitors, said capacitor dielectric material having a dielectric constant substantially higher than said second dielectric layer;

curing said capacitor dielectric material;

masking a dry film on areas of said second conductive layers where those are desired regions to form a copper layer thereon;

etching away exposed regions of said second conductive layers so as to form ground plane and power plane;

removing said dry film;

electroplating two copper layers respectively on said ground plane and power plane to seal said copper dielectric material to form built-in capacitors;

assembling and sintering said first conductive layer, said first dielectric layer, said ground plane, said second dielectric layer, said power plane, said third dielectric layer, and said third conductive layer together;

patterning said first conductive layer and said third conductive layer to form connective trace layers; and

performing a plating through hole process to connect said via holes to said connective trace layers and said power plane and ground plane.

2. The method of claim 1, further comprising at least one power ring and one ground ring on one of said connective trace layers, said at least one power ring and one ground ring respectively connecting to said power plane and ground plane.

3. The method of claim 1, further comprising filling another capacitor dielectric material into said via holes to form capacitors with different capacitance.

REMARKS

It is respectfully requested that the above amendments be made prior to calculating the filing fee. In this Preliminary Amendment, the claims are amended to correct typographical and grammatical errors, and the specification is amended to include a claim to priority under 35 U.S.C. §120 based on parent Application Serial No. 09/571,242. The Examiner is invited to contact the undersigned attorney at the number listed below if such a call would in any way facilitate examination of the application.

Respectfully submitted,

KINNEY & LANGE, P.A.

Date: August 23, 2001

By _____

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APPENDIX:
MARKED UP VERSION OF SPECIFICATION AND CLAIM AMENDMENTS

Please amend claim 1 as follows:

1. (Amended) A method of manufacturing built-in capacitors in [the] a multi-layer substrate, said method comprising:

forming a plurality of via holes in said multi-layered substrate, said multi-layered substrate comprising a first dielectric layer, a second dielectric layer, and a third dielectric layer, said second dielectric layer having two second conductive layers being respectively mounted on a top and a bottom surface to pattern as power plane and ground plane, said first dielectric layer, and said third dielectric layer having respectively [respective] a first conductive layer and a third conductive layer;

filling a capacitor dielectric material into a portion of said via holes, which are predetermined design as capacitors, said capacitor dielectric material having a dielectric constant substantially higher than said second dielectric layer;

curing said capacitor dielectric material;

masking a dry film on areas of said second conductive layers where those are desired regions to form a copper layer thereon;

etching away exposed regions of said second conductive layers so as to form ground plane and power plane;

removing said dry film;

electroplating two copper layers respectively on said ground plane and power plane to seal said copper dielectric material to form built-in capacitors;

assembling and sintering said first conductive layer[/], said first dielectric layer[/], said ground plane[/], said second dielectric layer[/], said

APPENDIX:
MARKED UP VERSION OF SPECIFICATION AND CLAIM AMENDMENTS

power plane[/], said third dielectric layer[/], and said third conductive layer together;

patterning said first conductive layer and said third conductive layer to form connective trace layers; and

performing a plating through hole process to connect said via holes to said connective trace layers and said power plane and ground plane.